

REMARKS

Claims 2-7, 9, 11-24, and 26-29 have been amended. Claims 1-30 remain in the application.

Typographical errors have been corrected in two paragraphs on page 13 of the specification. Paragraphs on pages 17 and 18 of the specification have been amended to conform them to the filed drawings (e.g., to FIGS. 8-10B) and to the remainder of the specification.

The Examiner objected to claim 22 because its language was similar to that of claim 18. The Examiner also objected to the dependency of claim 23. These claims have been amended to remove the objections.

The Examiner also objected to the lack of a proper antecedent in claim 26. This claim has been amended to provide the antecedent.

The Examiner rejected claim 1 under 35 USC §103(e) as being anticipated by Cho.

Applicants' independent claim 1 is directed to a reference signal generator that comprises:

an oscillator that provides an oscillator signal;

a buffer amplifier having an adjustable amplifier gain and coupled to process said oscillator signal into a reference signal that has a reference amplitude; and

a controller that adjusts said amplifier gain in response to said reference amplitude.

The Examiner stated that Cho, in his FIG. 1, discloses "a buffer amplifier [140] having an adjustable gain and coupled to process the oscillator signal into a reference signal [output from 140] that has a reference amplitude; and a controller [120, 130] that adjusts the amplifier gain in response to the reference amplitude".

In describing his FIG. 1, however, **Cho** states "the digital delay line 140 delays the external clock signal Clock according to the control signal from the counter and decoder 130" (column 1, lines 32-35). Because Cho teaches a device that delays a clock signal in accordance with a control signal, he fails to teach an amplifier that processes an oscillator signal into a reference signal with an amplifier gain that is adjusted by a controller.

Because he fails to teach an element of Applicants' independent claim 1, Cho cannot anticipate this claim. Because Cho teaches an entirely different device (a digital delay line), he teaches away from the elements of claim 1 and cannot, therefore contribute to a *prima facie* case of obviousness with respect to this claim. Because other cited art (Ooishi, Donnelly, Lin, Fiscus and Li) also fail to teach this element, they cannot support a *prima facie* case of obviousness with respect to this claim.

Independent claim 1 thus patentably distinguishes over the cited art. Because claims 2-10 add further limitations to claim 1, they also patentably distinguish over the cited art.

Applicants have amended independent claim 11 to differ from claim 1. Claim 11 also recites an amplifier that processes an oscillator signal into a reference signal with an amplifier gain that is adjusted by a controller. For reasons given above with respect to claim 1, the cited art fails to teach this element and cannot anticipate claim 11 nor support a *prima facie* case of obviousness with respect to this claim.

Independent claim 11 thus patentably distinguishes over the cited art. Because claims 12-25 add further limitations to claim 11, they also patentably distinguish over the cited art.

Applicants have corrected an antecedent error in independent claim 26. Claim 26 also recites an amplifier that processes an oscillator signal into a reference signal with an amplifier gain that is adjusted by a controller. For reasons given above with respect to claim 26, the cited art fails to teach this element and cannot anticipate claim 26 nor support a *prima facie* case of obviousness with respect to this claim.

Independent claim 26 thus patentably distinguishes over the cited art. Because claims 27-30 add further limitations to claim 26, they also patentably distinguish over the cited art.

Applicants therefore request reconsideration and withdrawal of the rejections and objections and an early allowance of claims 1-30.

Respectfully submitted,

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